REMARKS

This is responsive to the Office Action dated July 18, 2002 in which the Examiner rejects all the pending claims 1- 20 as either being anticipated by Utsu et al (US Patent No. 5,343,172) under 35 USC §102(b) or as being obvious over Utsu et al, or as being obvious over Utsu et al in view of Lleveland et al (WO 98/47190) under 35 USC §103(a). The Examiner also objects the Specification and the Drawings for formality deficiencies. The applicant has amended the Specification and Figure 5 to overcome the formality deficiencies. The applicant has also amended independent claims 1, 10 and 15 to more clearly define the present invention, and respectfully traverses the rejections as follows:

A brief explanation of the present invention is believed helpful in understanding the patentably distinguishing features of the present invention as claimed. The present invention teaches a novel circuit for input side impedance matching of a power amplifier. The circuit comprises an impedance transformer network to synthesize the predetermined impedance at the input of the power amplifier. In particular, as taught by the present invention, the impedance transformer network is joined in parallel with the source, and comprises a negative resistor in series with an inductor. By selecting the value of the negative resistor, the predetermined impedance is synthesized at the input of the power amplifier. The present invention solves the problems of reduced signal swing existing in the prior art where a LC match is utilized as the impedance transformer network or the matching circuit. The applicant does not believe that the present invention with the above emphasized distinguishing features explicitly defined in independent claims 1, 10 and 15 has been anticipated or implied in Utsu et al (US Patent No. 5,343,172), as explained in detail below.

Utsu patent teaches a variable reactance circuit utilized in a variable matching circuit to realize post-adjustment at a low loss. As most clearly shown in Figures 1 and 2A-2C, the variable reactance circuit in Utsu, which is parallel connected to the amplifier, basically comprises an

inductive load 22, 142 which is connected to the drain of a FET transistor 21, 141. The inductive load 22 is equivalent to a resistive component 222 in series with an ideal inductance 221. The FET transistor 21 is equivalent to have a negative resistive component 211 and a gate-source capacitor 212. The negative resistor component 211 cancels out the resistive component 222 of the inductive load, thus realizing a low loss in the matching circuit. The adjustment of the reactance of the matching circuit is realized through the bias voltages applied to the EFT, which will change the capacitance of the gate-source capacitor 212, thus changing the reactance of the whole matching circuit.

However, the Examiner appears to have misread the variable reactance circuit as the variable matching circuit in the Utsu patent, and therefore misread it as the impedance transformer in the present invention which synthesizes the predetermined impedance at the input of the amplifier. The variable reactance circuit, which is designated as 14 in Figure 1 and which is separately shown in Figures 2A-2C, only constitutes a part of the variable matching circuit which further includes a reactance element connected in series with the amplifier (12 in Figure 1, 31 in Figure 3 and 44 in Figure 4). It is clearly described in Utsu et al that this reactance element (12, 31 and 44) constitutes the variable matching circuit together with the variable reactance circuit. For example, it is explicitly described in col. 5, lines 13-16 that "an input matching circuit constituted by a series reactance 44 and a parallel variable reactance circuit 45 is connected to the gate electrode of the FET 41"; in col. 4, lines 58-61 that "... when a variable reactance circuit 32 is set and parallelly combined with a series reactance 31, a variable matching circuit having a very low loss can be constituted like..."; and in col. 3, lines 53-54 that "the matching circuit is thus constituted by the reactance circuits 12 to 15". Therefore, the variable reactance circuit is not the matching circuit itself. In other words, the variable reactance circuit does not synthesize the predetermined impedance at the input of the amplifier. In fact, the matching circuit in Utsu is a LC match, and what taught in Utsu et al patent is an improvement in a LC match by providing a variable reactance circuit as a variable "inductor" in the

LC match. As explained in the present application, an LC match has a problem of reduced signal swing which is solved by the present invention.

The applicant has amended independent claims 1, 10 and 15 to more clearly and precisely define the present invention, and believes such amendment will clearly distinguishes the present invention from the cited Utsu et al. In particular, the variable matching circuit in Utsu, which corresponds to the impedance transformer network in the present invention and which also synthesizes the predetermined impedance at the input of the amplifier, is not parallel to the amplifier or source because of the series reactance element (12, 31, 44) in its LC match. The variable reactance circuit, as misread by the Examiner as the impedance transformer network of the present invention, does not synthesize the predetermined impedance at the input of the amplifier. Therefore, the present invention defined in independent claims 1, 10 and 15 are not anticipated by the cited Utsu et al patent.

Furthermore, in both independent claims 10 and 15, it is further defined that "a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier". This feature can not be found anywhere in Utsu et al. In Utsu, the negative resistive component of the FET transistor serves to cancel out the resistive component of the inductor so as to realize a low loss in the variable reactance circuit. Utsu never teaches to select a value of the negative resistive component in the FET to synthesize the predetermined impedance. In fact, Utsu even does not teach to select the value of the negative resistive component but only states that "the value of the negative resistive component depends on the value of the inductance component of the inductive load" (col. 2, lines 60-62). Therefore, this distinguishing feature further strengthens the patentability of claims 10 and 15. For the same reason, the patentability of claim 4, which is dependent to claim 1, is also strengthened.

At least for the same reasons, the applicant believes the dependent claims 2-9, 11-14 and 16-20 are also patentable.

The applicants therefore respectfully request reconsideration and allowance in view of the above remarks and amendments. The Examiner is authorized to deduct additional fees believed due from our Deposit Account No. 11-0223.

Respectfully submitted,

KAPLAN & GILMAN, L.L.P.
900 Route 9 North
Woodbridge, New Jersey 07095
Telephone (732) 634-7634

Dated: October 18, 2002

Jeffrey I. Kaplan
(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231 on October 18, 2002.

Dated October 18, 2002 Signed Paula M. Halsey Print Name Paula Halsey

MARKED-UP VERSION OF THE AMENDMENT

IN THE SPECIFICATION:

On page 7, the paragraph at lines 3 -11:

In most cases, impedance at the input side of a power amplifier can be modeled as a resistor 56 having a value R 68 in series with a capacitor 58 having a capacitance **[–jxc70]** –jXc 70. As will be described in further detail below, impedance transformer network 50 matches the input side impedance by "synthesizing" the source side impedance. This is generally accomplished by choosing a proper value R1 64 for negative resistor 52 (described in further detail below) and then setting inductor reactance 66 equal to the capacitance **[58]** 70 of the electronic device at a required frequency of operation. Using this technique, any impedance can be synthesized across nodes A 60 and B 62.

On page 7, please amend the paragraph at lines 16 - 19 as follows:

Where MAG[*Zeff*] is the magnitude of effective impedance synthesized at the input side (i.e., across nodes A 60 and B 62), R1 is the value of negative resistor 64, R is the value of resistor 68, and X is the capacitance 70 of the electronic device at a required frequency of operation and the inductor reactance 66 as well.

IN THE CLAIMS:

1. (Amended) A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance; and

an impedance transformer network <u>to synthesize the predetermined impedance at an input of the power amplifier;</u>

<u>wherein the impedance transformer network is</u> joined in parallel with the source, [wherein the network] <u>and</u> comprises a negative resistor in series with an inductor[, and wherein the network synthesizes the predetermined impedance at an input of the power amplifier].

10. (Amended) A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance;

an impedance transformer network <u>to synthesize the predetermined impedance at an input of the power amplifier, said impedance transformer network being</u> joined in parallel with the source[, wherein the network comprises] <u>and comprising</u> a negative resistor in series with an inductor; [and]

wherein a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier, and wherein the inductor has a reactance equal to a capacitance of the device at a required frequency of operation.

15. (Amended) A method for matching impedance at an input of a power amplifier in an electronic device, comprising the steps of:

providing a signal from a source, wherein the provided signal has a predetermined impedance;

joining an impedance transformer network in parallel with the source <u>to synthesize</u>

~~the predetermined impedance at an input of the power amplifier~~, wherein the network comprises a negative resistor in series with an inductor; and

selecting a value for the negative resistor so that the predetermined impedance is synthesized at the input of the power amplifier.